

Figure 1:

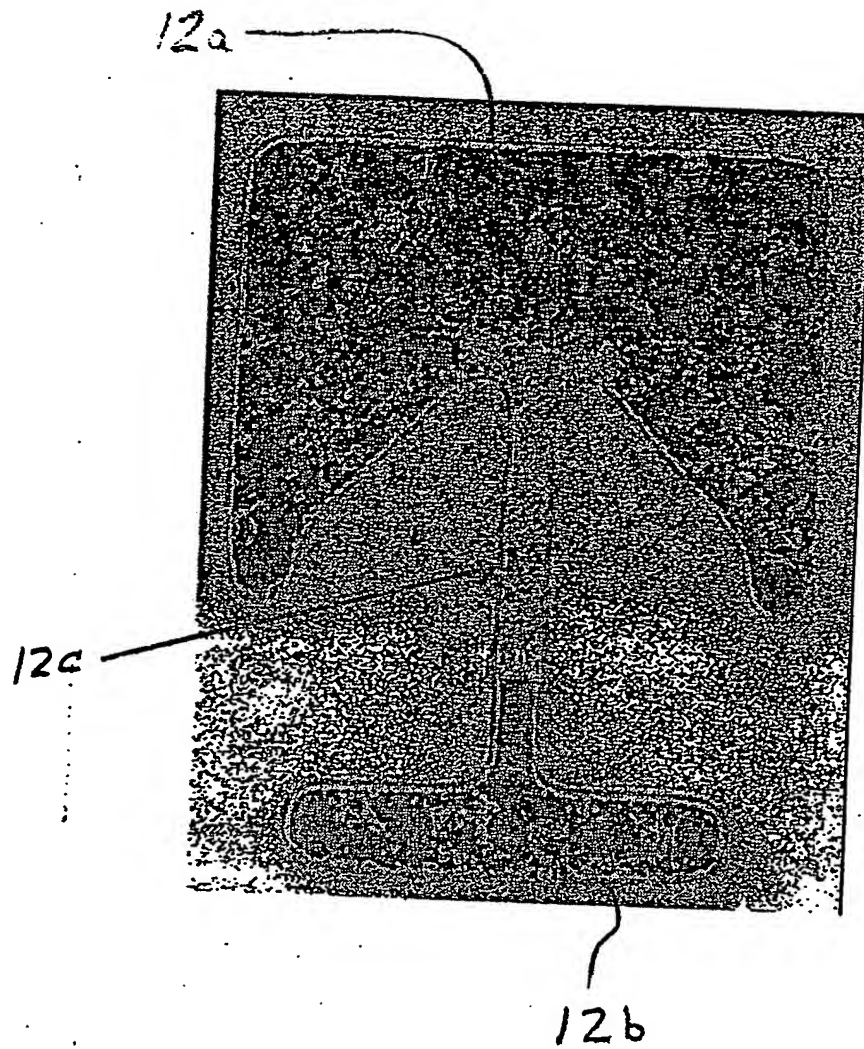


Figure 2:

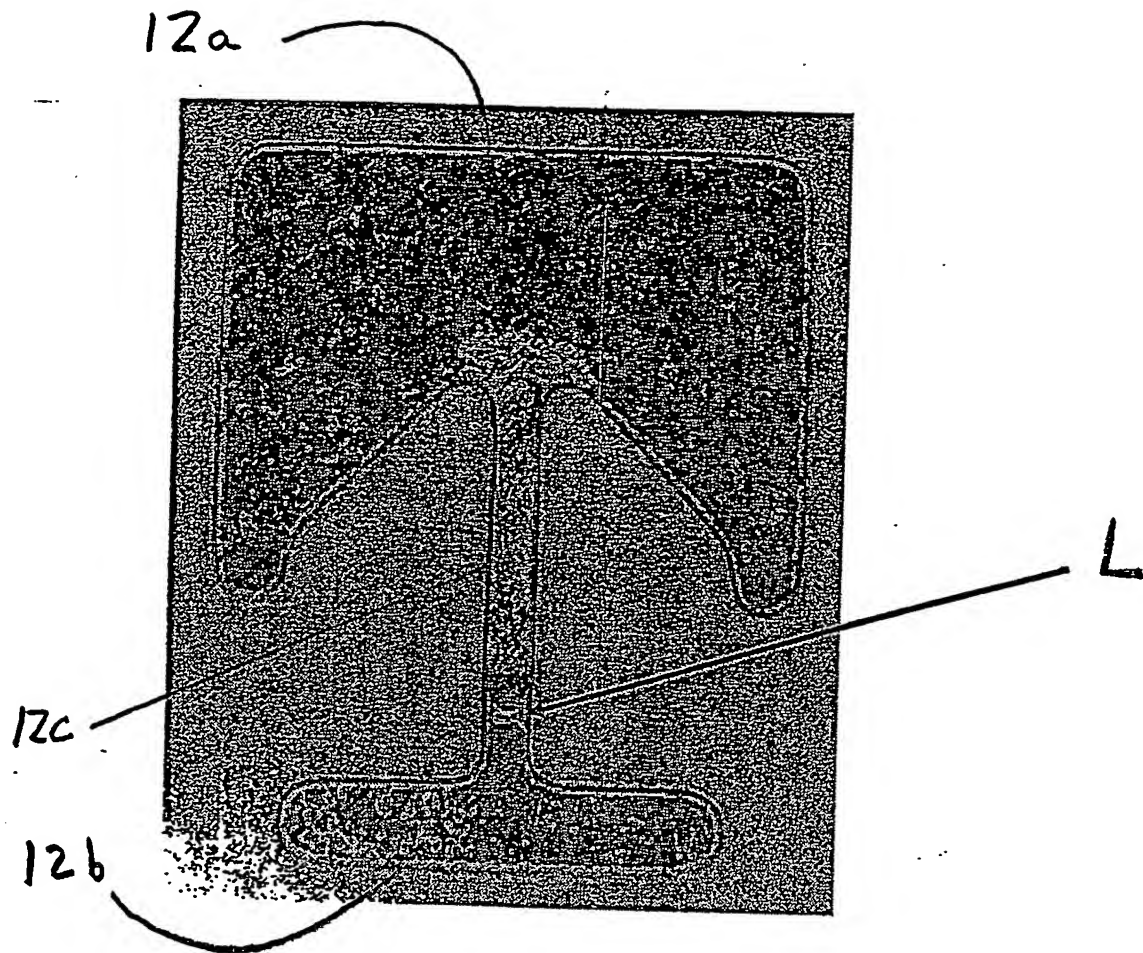


Figure 3:

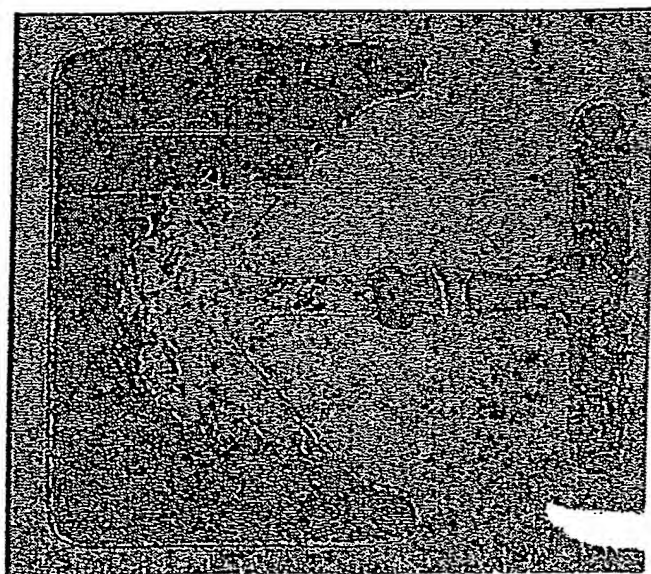


Fig. 4 (a)

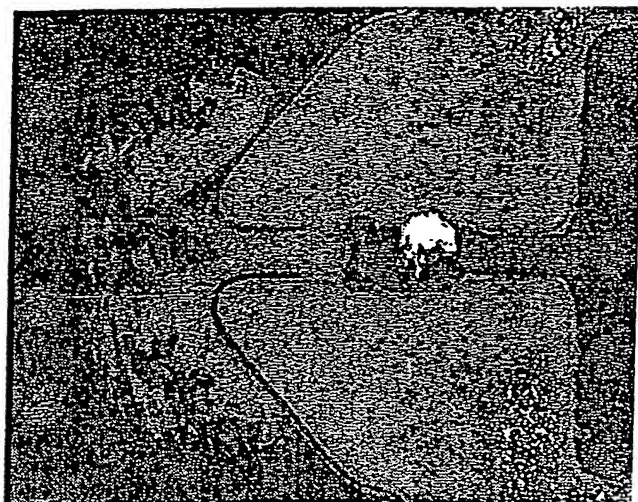


Fig. 4 (b)

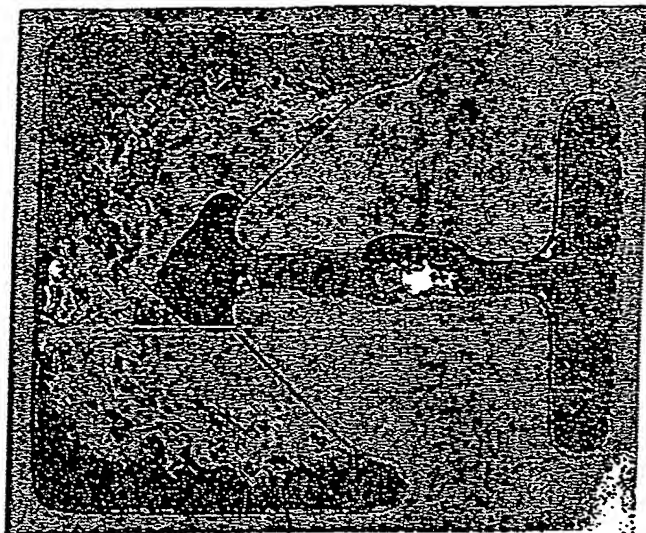


Fig. 4 (c)

Figure 4:

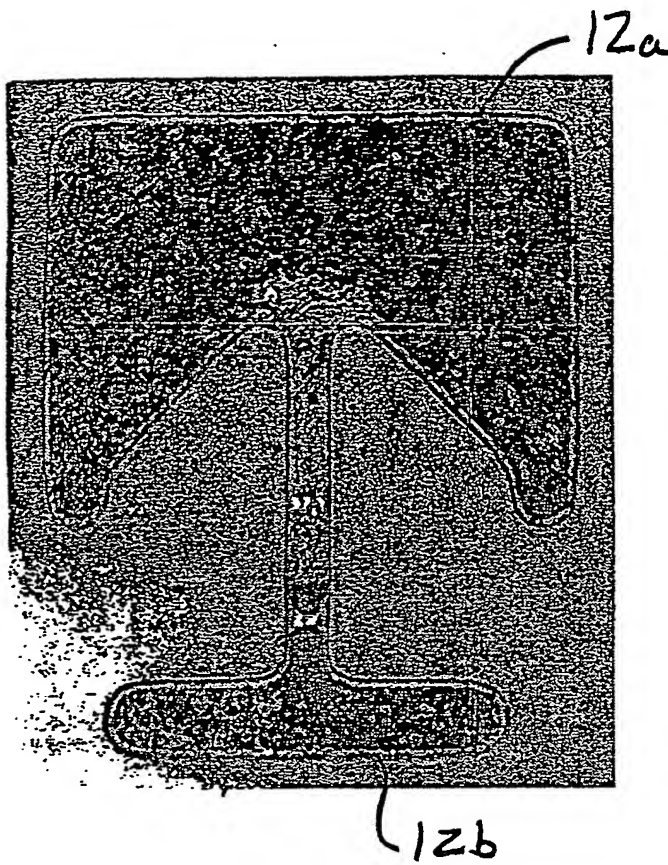
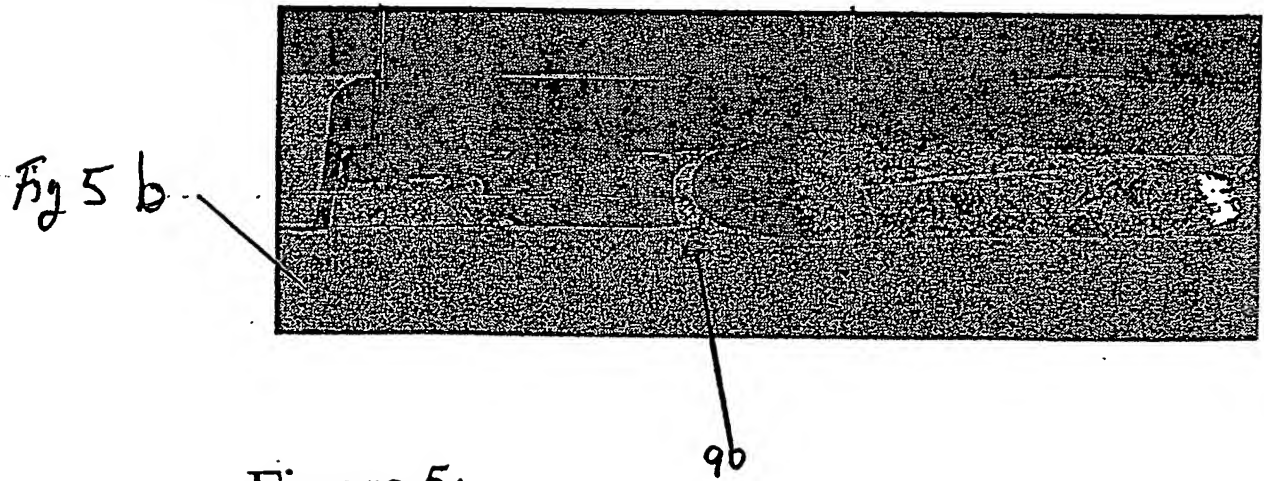


Fig 5 a



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Figure 5:

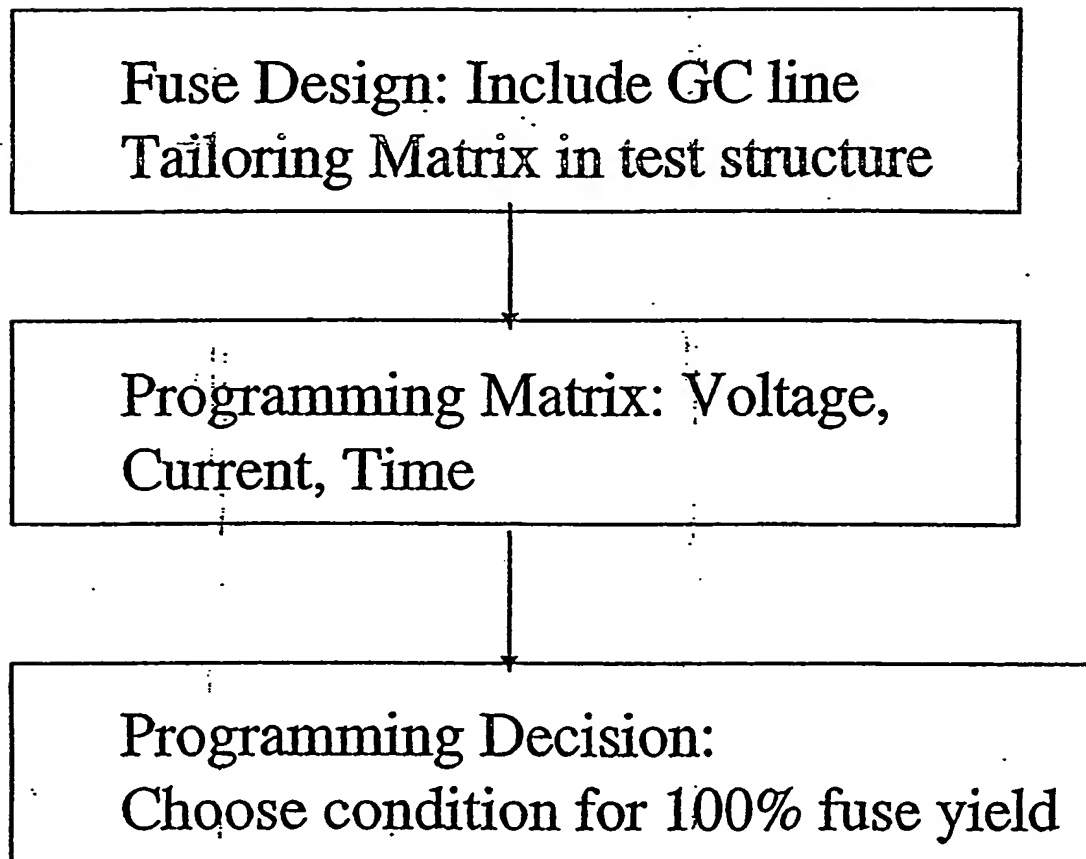
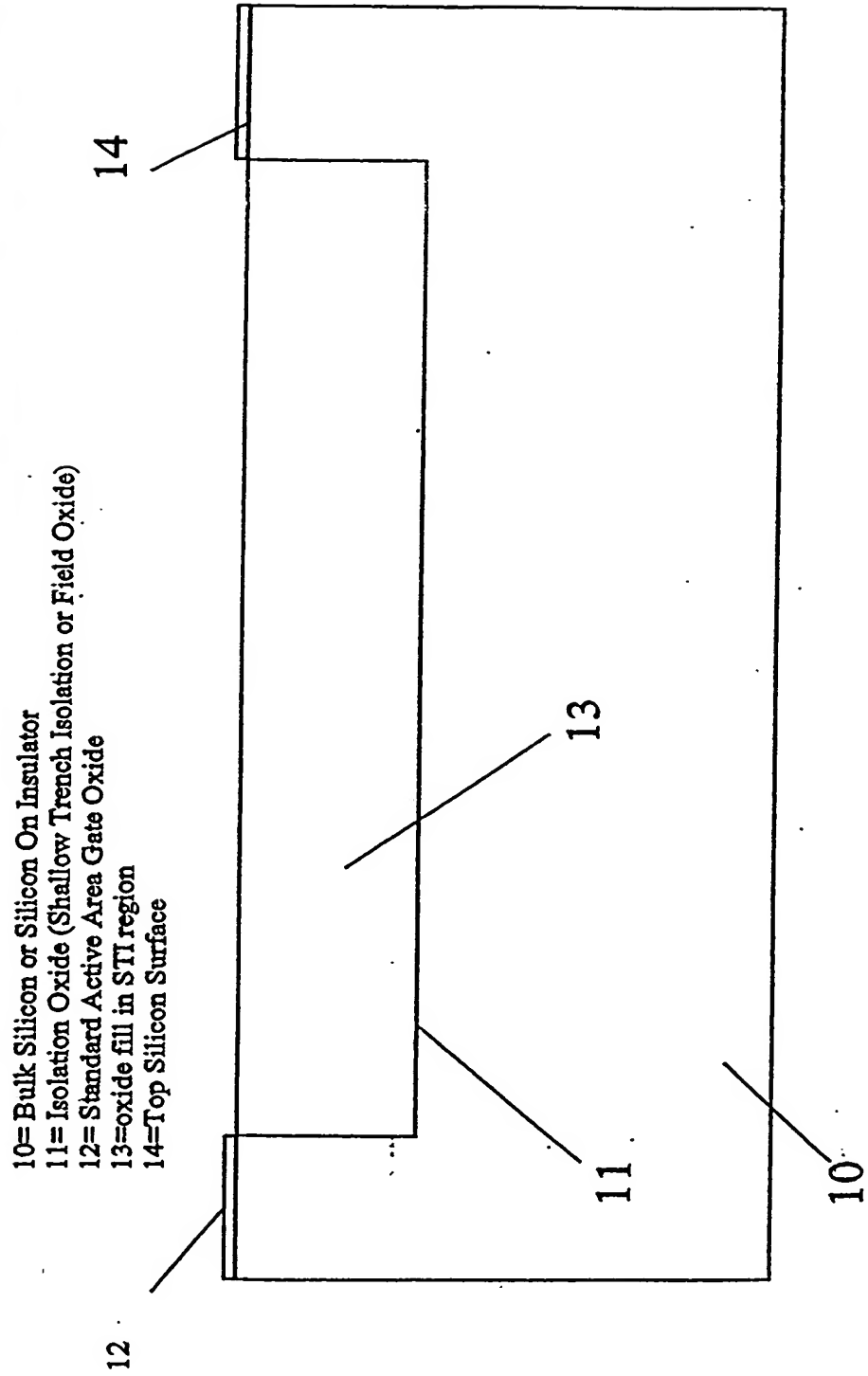
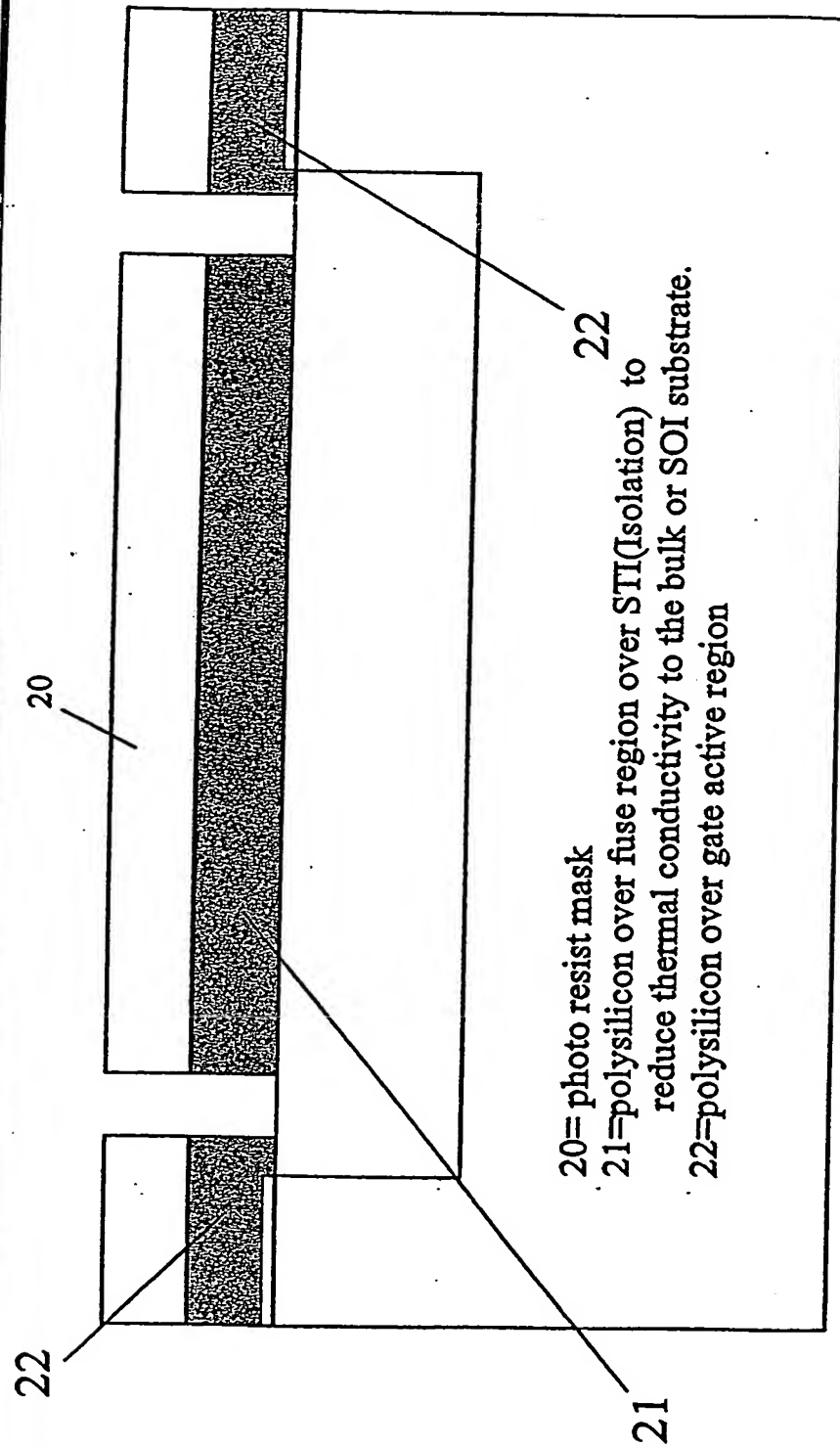


Figure 6

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Figure 1: Starting Bulk or SOI wafer: Thin oxide / Isolation Regions formed



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Figure 2: Deposit / Pattern Polysilicon

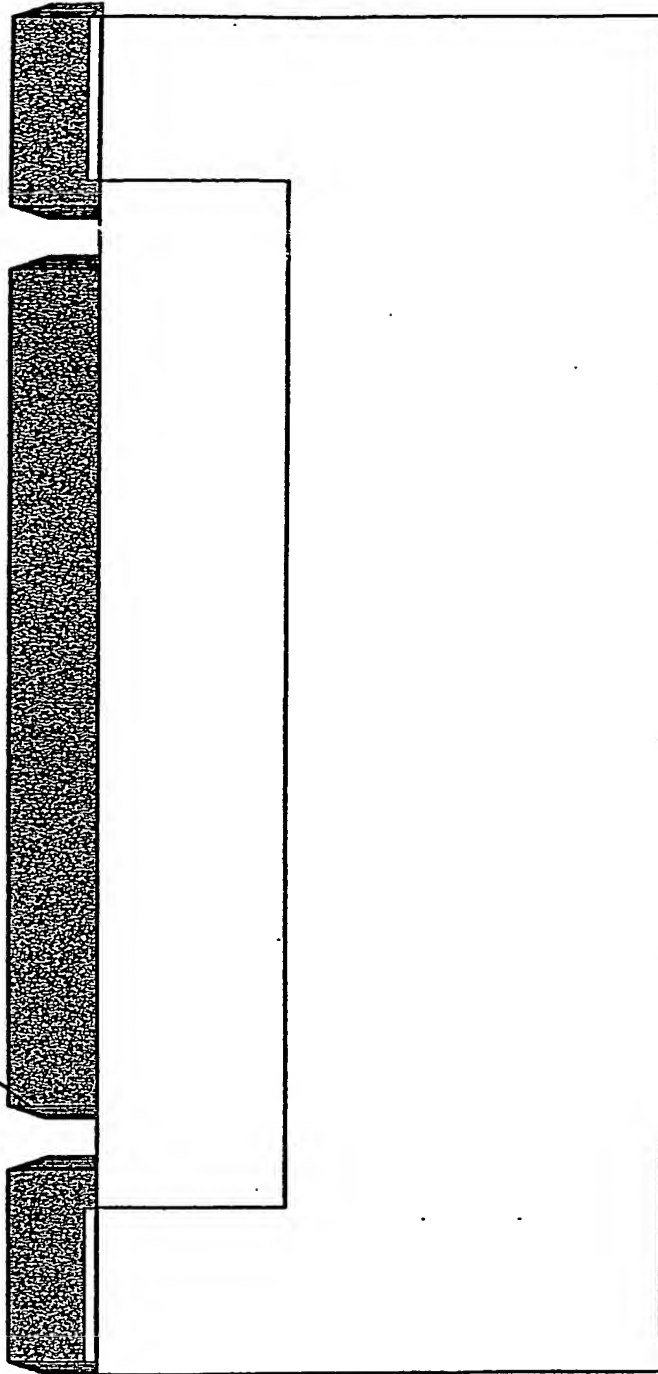


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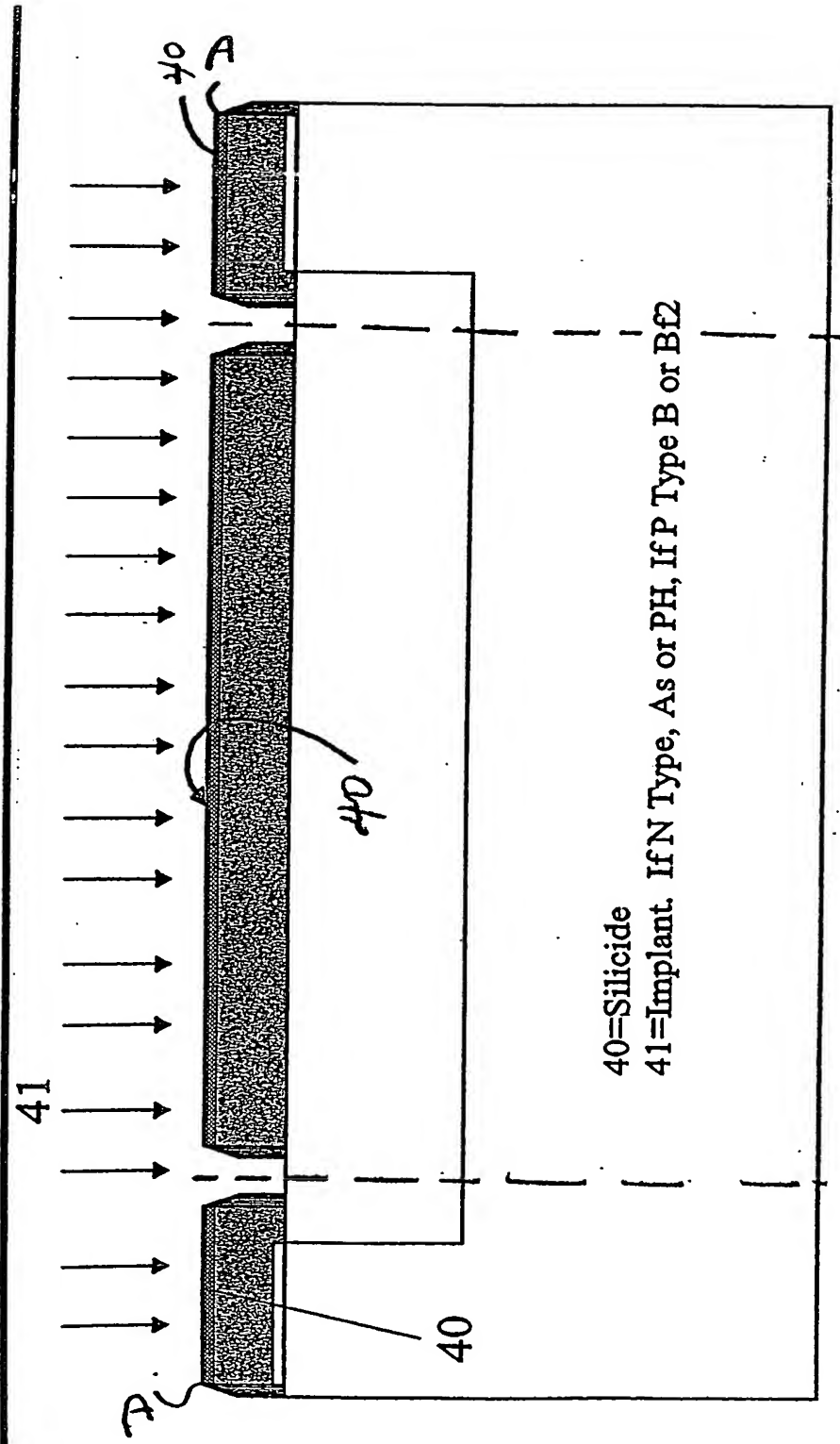
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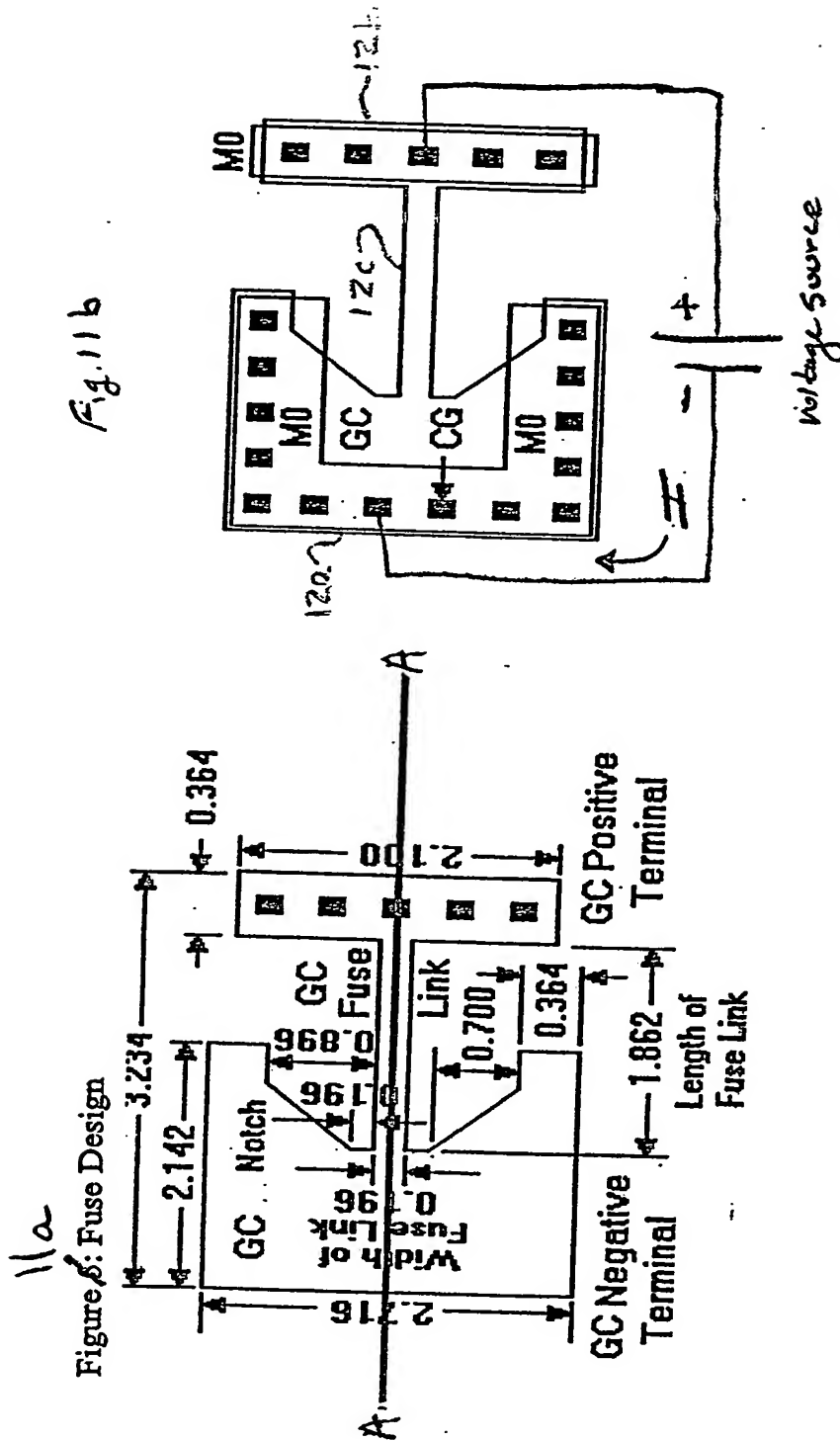
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Figure 3: Form Sidewall Spacers

30= Sidewall Spacer Formation

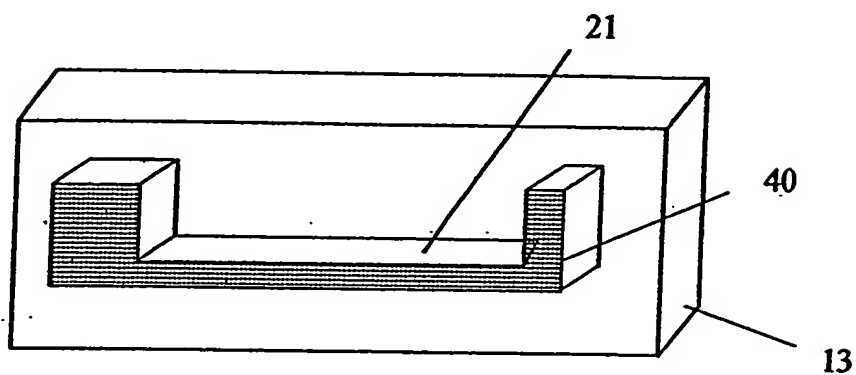


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Figure 4: Implant Gate / Source / Drain / E-Fuse region Silicide Gates (If not In-Situ Doped Polysilicon)

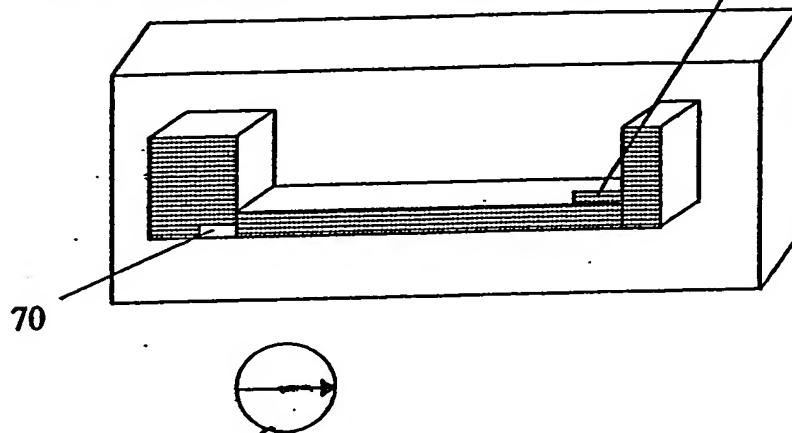




¹²
Figure 6: Fuse Cross Section A - A Prior to programming

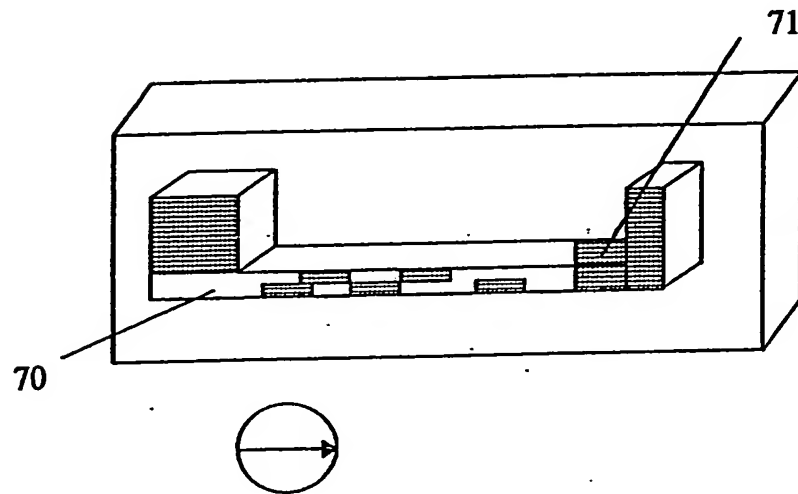


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Figure 7: Fuse Cross Section A - A During Programming 71



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Figure 8: Fuse Cross Section A - A Just prior to programming



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Figure 9: Fuse Cross Section A - A Programmed device

